Exploring Partial Reconfiguration for Mitigating SEU faults in SRAM-Based FPGAs
Cristiana Bolchini, Fabio Salice, Marco D. Santambrogio
Dip. Elettronica e Informazione - Politecnico di Milano - ITALY

Methodology Goal:
The aim of our work is the exploitation of partial dynamic reconfiguration in order to mitigate the effects of radiation-induced faults, such as Single Event Upsets (SEUs).

The adopted fault model:
Radiation induced errors in microelectronic circuits caused when charged particles lose energy by ionizing the medium through which they pass, leaving behind a wake of electron-hole pairs. These faults are transient and non-destructive: Single Event Upsets & Single Event Transient

The Reconfiguration for Reliability:
Application of partial reconfiguration, exploiting the benefits of on-line fault detection to identify the occurrence of a SEU; such information is used to localize the portion of the FPGA to be re-configured to recover from the error by dynamically performing partial reconfiguration. All information on fault localization and the part to be re-configured are computed at design time, and stored in an opportunely hardened memory, to be used when, and if, a fault occurs.

The strategies are part of the library of techniques among which the designer can select the most promising one, according to his/her requirements and to the reconfiguration possibilities offered by the family of FPGAs adopted as target platform. Together with the proposed techniques, also classical ones (such as the one found in literature) are considered, to cope with boards unable to support partial dynamic reconfiguration.

Proposed Design Strategies:

Spare logic reconfiguration
A portion of the entire system (e.g., the critical section) is replicated and compared continuously, whereas the sub-blocks of remaining part of the system are cyclically monitored, for a period of time depending on the configuration time and the amount of blocks, by means of opportunely reconfiguring the spare logic with a scheduled round robin policy; in this way, all the sub-parts of the non critical system are periodically monitored.

Duplication & Comparison
The duplication with comparison strategy is adopted to identify the occurrence of a SEU and to trigger a reconfiguration of the affected frame of the FPGA. The entire specification has to be partitioned into a set of subsystems. Each portion has its own fault detection signals; when a fault is detected the portion of the FPGA controlled by those signals is reconfigured to mitigate the fault effect.

Dual-FPGA
The architecture exploiting a Dual-FPGA platform approach, coupled with Triple Modular Redundancy and partial reconfiguration, constitute another adopted design strategy. The approach is similar to the one presented in [Mitra et al., 2004] as it uses two FPGAs, but improves reconfiguration time, and thus performance, by exploiting the partial reconfiguration of the module that has produced a minority output.

Multiple-FPGAs
Architectural solution based on the use of a set of FPGAs connected so to implement the desired functionality. Each FPGA implements a single sub-system block and, from the I/O point of view, any FPGA always returns a fault-free value resulting from a voter evaluation. More specifically, each FPGA implements a TMR for the sub-system so that, when inside a FPGA an error is identified, the reconfiguration mechanism is activated in order to restore the correct functionality.

Different strategies are proposed to cope with SEU faults, affecting either the configuration memory elements or the data registers of the FPGA. The different approaches can be qualitatively compared in terms of costs and benefits to allow a selection of the most appropriate solution based on constraints and requirements.

http://www.dresdg.org/?q=r4