PARTIAL DYNAMIC RECONFIGURATION: THE CARONTE APPROACH.  
A NEW DEGREE OF FREEDOM IN THE HW/SW CODESIGN.

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ABSTRACT

The design of embedded systems is rapidly changed during 
the last decade. It is possible to identify two main factors 
that are involved in this process: HW/WS codesign and 
dynamic reconfigurable architecture. This work aims at 
introducing an innovative methodology that allows to easily 
implement on an FPGA a system specification, taking as in-
put its high-level description, such as C or SystemC, and 
exploiting the capabilities of partial dynamic reconfigura-
tion and HW/SW codesign methodologies. In order to meet 
the software requirements of complex systems, the solution 
is also provided with the porting of a real-time GNU/Linux 
OS, CLinux, which allows software processes to exploit a 
rich set of features, and with a Linux module that simplifies 
the handling of reconfiguration.

1. RATIONALE

Emphasis is given on correctness and dependability of join-
ing technologies in the hardware and software domains, on 
the reconfigurable hardware characteristic, on the satisfac-
tion of real-time constraints and, in general, on the explo-
ration of the solution space, in order to evaluate the most 
effective solutions that are compatible with the design and 
market constraints. These goals can be reached with the 
definition of families of platforms, which can be customized 
and configured to effectively implement the required vari-
ety of applications. In the factory automation and telecom-
unication fields, platforms address the continued growth in 
the network bandwidth and services, the continuous intro-
duction of new protocols, and the necessity of adapting to a 
variety of standards and application environments.

The Caronte project proposes an alternative approach for 
embedded design flow binding HW/SW codesign and 
hardware reconfiguration to focus the design attention on 
the entire platform characterization instead of the singlepro-
cessing element. This project envisions the development of 
new tools and the identification, formalization of new mod-
els and design methodologies that can represent and imple-
ment embedded system able to cope with new system re-
quirements. It proposes a design methodology, as shown in 
Figure 1, for dynamically reconfigurable systems providing 
a dynamic architecture that, thanks to the processor embed-
ded in the FPGA, is able to dynamically change the design 
implementation to meet the requirements of the system im-
plementation.

Fig. 1. Caronte Flow Overview

The methodology provides a solution for the partial dy-
namic reconfiguration of an embedded system, using a com-
mon FPGA and development board, without any specific or 
dedicated device trying to provide to the designer a complete 
methodology that strongly decreases the time to market of 
the final implementation of the system.
1.1. Caronte innovations

The Caronte project will enhance mainly three key aspects of the design of embedded system. System modeling and characterization currently lacks a description framework when HW/SW codesign, dynamic hardware reconfiguration and networked architectures become all central to the embedded system design. Caronte aims at creating a framework for evaluating the performance of a system implementation providing to the designer a set of tools that will help him during his work. Starting from a C or a SystemC description able to describe both the software and the hardware components of the system the Caronte framework will provide: (a) a SystemC dynamic reconfigurable model of the system description; and (b) a set of different metrics oriented to the HW/SW codesign, such as channel communication estimation, profiling information, or to the hardware dynamic reconfiguration. There is still lack of a complete and homogeneous support for dynamic reconfiguration within a standard operating system. In our methodology, the use of a complete operating system, such as the Linux kernel, is a major advantage, since the hardware management functions are all demanded to the operating system, and user processes can access the devices using an easier interface. Moreover, many different applications can be run at the same time on the processor thanks to the multitasking provided by the operating system and can share the resources mapped on the FPGA. Methods and tools for applications mapping of descriptions and models provided using High Level Languages, such as C or SystemC currently lacks the ability of effectively customising an application onto a platform. They are not able to estimate the expected performance of alternative HLL-to-embedded-system transformations and of the real-time and dependability characteristics. Without such precise estimations, it is not possible to find a feasible solution into the solution space that can best fit the problem under examination. The Caronte project design framework implements an innovative problem-model-system mapping methodology, since it implements the following analysis: (a) generation of an intermediate representation, IR, of the system independent of the description language used to describe the system; (b) evaluation of the expected performance of the application based on the different metrics applied on the IR of the system.

2. CURRENT WORK

The analysis of the state of the art has shown that there is still lack of a complete and homogeneous support for dynamic reconfiguration within a standard operating system, allowing to access reconfigurable devices transparently for the processes running on the system, exactly as with usual peripherals and resources of the system. Dynamically configurable peripherals, [1], introduce also an interesting opportunity for a PnP management system, which performs driver loading for the specific kind of device. The HW side of the infrastructure is based on the Caronte system, [2, 3], where a methodology for the design of a complete embedded system which makes use of dynamic reconfiguration capabilities is presented. From the SW point of view, the proposed infrastructure presents a different approach than the Caronte one. The latter consists in a standalone system running a SW controller on the processor. This application contains a scheduler which manages the allocation of FPGA areas to the different reconfigurable SW components. The new methodology, instead, aims at integrating the peripheral management in the operating system. This allows a broader variety of applications, but also maintains the possibility of implementing the Caronte SW solution as a userspace application. The proposed solution is not bound to a specific FPGA vendor or family of reconfigurable devices, but can be considered as a middleware between the SW applications and the reconfigurable peripherals, [1, 3], where the upper side of the middleware is totally HW-independent and does not require any modification among different platforms, and the lower side only requires few adjustments according to the different HW platforms used for partial reconfiguration.

Tests have shown that introducing an operating system able to support also the self dynamic reconfiguration is not so expensive in what concerns the amount of the hardware resources usage. The set of tests has been implemented using the same architecture as the one proposed for the Virtex II Pro xc2vp7 but using a Xilinx FPGA, the Virtex II Pro xc2vp20, that is characterized by a greater number of hardware resources and a bigger reconfigurable area. On this new FPGA we were able to implement a self dynamic reconfigurable system using an operating system with better performances from reconfiguration time point of view.

We made different tests using the proposed software solution and the Caronte architecture and the reconfiguration performance has been estimated in about 1.5 MBytes/s transfer rate.

3. REFERENCES

