Politecnico di Milano
DRESD Project

RECONFIGURATION 4 RELIABILITY

2007

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1 Involved People

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2 Project Introduction

The adoption of Field Programmable Gate Arrays (FPGAs) as a platform for the development of embedded systems is nowadays common practice, to benefit from the limited costs, the highly flexible architecture, as well as the possibility to re-program it to modify its behavior or to correct it in case of problems. In particular, this opportunity to re-program the device has received a lot of attention and improvements have been introduced to support such a feature also *dynamically* (i.e., at run-time) and *partially* (i.e., applied to only a portion of the device). These new features make it possible both to reduce the time necessary to re-program the device and to avoid the necessity to halt the entire system [1, 2].

On the other hand, the flexibility of this specific platform provided by the reconfiguration capability constitutes also a problem, since the SDRAM memory elements storing the configuration bitstream (as well as the other memory elements of the device) are susceptible to radiation-induced temporary faults, also called soft errors or Single Event Upset (SEU), which corrupt the memory content causing the system to misbehave. In order to cope with this problem, particularly significant for the space environment but always more and more relevant also at ground level, fault detection and tolerance techniques need be introduced.

In this scenario several studies have been carried out to deal with the problem of radiation-induced faults in SRAM-based FPGAs from different points of view [3, 4, 5, 6, 7, 8, 9]; some of them apply well-known techniques, traditionally adopted for other platforms too, focusing the attention on the peculiarities of the selected platform, while others exploit the opportunities of reconfiguration to mitigate faults effects. Given the available solutions, the design of a reliable system on SRAM-based FPGAs may be achieved in different ways, according to the designer's requirements and constraints.

The main contribution of Reconfiguration 4 Reliability project is the definition of a methodology supporting the design of reliable FPGA-based systems. In particular, the methodology aims at providing a framework for the design of reliable systems also by exploiting partial dynamic reconfiguration and for assessing system reliable properties by means of fault injection.

3 Motivations and Goals

Reconfiguration 4 Reliability approach aims at designing reliable systems implemented on FPGAs, able to cope with the effects of faults caused by radiations. The approach consists in applying well-known fault detection/tolerance techniques, such as Triple Modular Redundancy (TMR) or Duplication With Comparison (DWC), coupled with partial dynamic reconfiguration in order to identify and mitigate the occurrence of a SEUs. The idea is to exploit standard techniques for detecting bit-flips and classifying them as temporary errors, i.e., occurring in application data storage units or permanent errors, i.e., affecting configuration memory. While the first case may be recovered by resetting the system, the second one requires a reconfiguration of the faulty memory portion.

The project proposes the study of a methodology for the design of reliable FPGA-based systems by exploiting the presented technique.

4 Project Description

The proposed methodology for the FPGA-based system design is composed by three may tasks:

- methodology for reliable reconfigurable systems design;
- design of Totally Self-Checking components;
- design of a fault injection environment.

First two tasks are related to the study of a design flow for reliable systems and aim at proposing both methodologies for applying reliability techniques and studying new techniques and reliable components. The second part deals with reliability assessment and aims at proposing a fault injection platform.

4.1 Methodology for reliable reconfigurable systems design

The first activity of the project aims at studying a methodology for designing a reliable implementation of a system by means of the adopted technique, i.e., partial dynamic reconfiguration coupled with standard fault detection/tolerance techniques (TMR or DWC).

In order to apply the adopted technique, the system should be partitioned into modules; in fact, the technique is independently applied on each module. When considering the partitioning task, on one hand there is the solution where the system is not partitioned and is monitored only on the primary outputs (corresponding to a complete reconfiguration solution), and on the opposite hand there is a partitioning with comparison of every single functionality. In between there are several alternatives, each one characterized by its costs and benefits. More precisely, the size of such subsystems determines the precision of fault localization and some considerations need be introduced: i) the localization capability grows with the number of subsystems independently controlled; ii) the area overhead grows with the number of subsystems independently controlled; and iii) it is necessary to be able to control the process so that the identified subsystems are placed in separately reconfigurable portions of the device. Different partitioning solutions for the given device lead to alternative designs characterized by different costs due to the varying number and size of the comparators and the amount of shared logic. For instance, Figure 1 shows some solutions obtained by applying TMR at different levels of granularity.

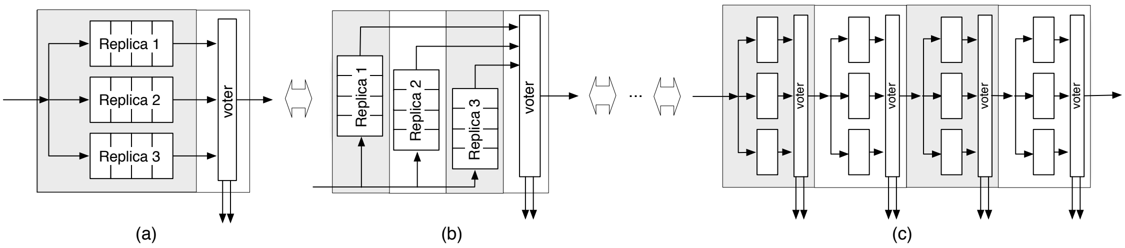

Figure 1: TMR applied with different levels of granularity.

Some solutions may not be interesting; considering the situation depicted on the left of Figure 2 the benefits of knowing precisely which module (a replica of f_1 or a replica of f_2) is faulty is not significant since the entire portion will be re-configured. As a result the first voter could be avoided allowing a more limited area overhead with the same coverage and partial reconfiguration control.

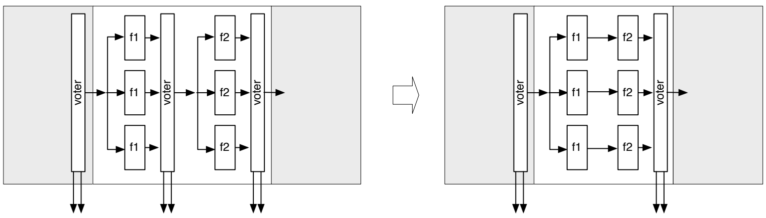

Figure 2: Disadvantageous partitioning solution.

The methodology [10] aims at estimating the costs and benefits deriving from the possible different partitioning solutions. This exploration of the solution space is based on several metrics estimating several features such as i) size of the subsystems (used to estimate area and ro-indices), ii) size of the data widths to be compared (used to derive the size of the comparators), and iii) amount of the minimal reconfiguration portion of the FPGA (used to derive available area and reconfiguration times). Figure 3 shows methodology flow. A preliminary synthesis of the initial device partitioned into subsystems is performed, to identify the basic costs to perform the estimations. Starting from this finer-grain partitioning, incremental aggregation of modules is performed to find a satisfying trade-off between area overheads and partial reconfigurable times.

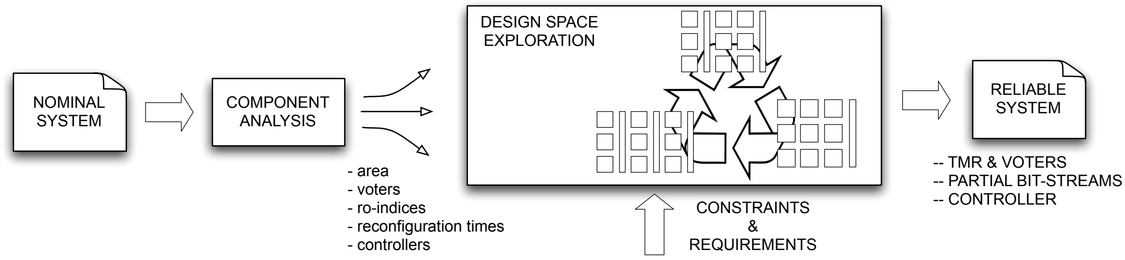

Figure 3: Design space exploration flow.

4.2 Design of Totally Self-Checking components

The design exploration framework requires a repository of standard Total Self-Checking (TSC) components to be used during the implementation of the reliable version of the system description. Considering particular features of FPGA devices, sometimes standard components studied for ASIC design are not effective on the adopted device; other components may be better re-designed or adapted to the FPGA features and architecture. Finally, new components dealing with partial reconfiguration issues must be designed. Example of required TSC components are voters, checkers or controllers.

4.3 Design of a fault injection environment

The last activity of Reconfiguration 4 Reliability deals with approaches for reliability level assessment. In particular, it pursues the goal of implementing a fault injection platform for analyzing fault effects and the effectiveness of the applied fault detection/tolerance techniques.

The idea is to implement a platform, based on a FPGA, that allows execution freeze and the modification of application status or configuration. In order to enable these features the platform should provide asynchronous start and stop commands, and modification of configuration and application status by means of partial dynamic reconfiguration. The platform should provide also features for the readback of FPGA content.

Important issues to be considered for platform implementation are:

Observability : system status must be observable, both configuration and application status.

Controllability : injected fault must be controllable, i.e., it is necessary to be able to specify precise fault location and injection time.

Non intrusiveness : in order not to introduce variations and additional elements that are not part of the system under consideration

Efficinency : additional features, such as check-point store and retrieve, should make simulation more efficient.

5 General information

- Webpage: www.dresd.org/?q=r4r
- Mailing List: r4r-ml@dresd.org
- To have more information regarding Reconfiguration 4 Reliability: r4r@dresd.org
- For a complete list of information on how to contact us: www.dresd.org/?q=contact_r4r
- Related work - wiki: www.dresd.org/?q=soa_r4r

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