.:: DRESD Projects :::

Caronte

Caronte aims at introducing a complete methodology that allows to easily implement on an FPGAs system a specification by exploiting the capabilities of partial dynamic reconfiguration provided by the modern devices. The Caronte design flow can be used to implement a system using different FPGAs exploiting different reconfiguration techniques, allowing the designer to modify its intermediate results or to leave the entire design process to the Caronte framework.

CITiES

The Communication Infrastructure Tailored to Embedded Systems design (CITiES) project aims at defining a complete methodology for the exploration of the solution space of the CIs (point-to-point, bus, Network-on-Chip, with their parameters), in order to support the designer in the choice of the best fitting CI.

DReAMS

Multi-FPGA systems introduce interesting and novel challenges in the definition of more complex and powerful reconfigurable systems. DReAMS aims at developing a general high-quality complete workflow (from the specification to the bitstreams creation through portioning and synthesis) capable of producing designs without the intervention of a human operator during its several phases. The design workflow deals with the creation of multi-FPGA systems that are implemented on physical FPGA ensembles; for this reason a branch of the project deals with the creations of such architectures using low cost devices.

OSyRiS

The design of an Operating System solution able to support and manage the reconfiguration both in a SoC or in Multi-FPGAs scenario without changing the designer interaction with the developing framework. Due the Multi-FPGAs scenario it is also mandatory to design a solution able to support both an internal and an external reconfiguration hiding this process to the system designer. Those are all aims of the OSyRiS project.

Polaris

The context where Polaris finds its rationale, is a self, partial and dynamical reconfiguration scenario, in both its *mono-dimensional* and *bi-dimensional* paradigms. Goal of Polaris is the creation of a complete workflow to help the designer in the creation and management of self partially and dynamically reconfigurable systems. The provided support is related to the definition of area constraints for tasks, the creation of an efficient runtime task allocation manager and finally the generation of a solution to obtain internal and fast relocation of tasks.

R4R

This project takes its first steps from the opportunity to put together the experience of the past years in the design of digital systems with dependability properties and the fast evolving research in the field of dynamic reconfiguration of FPGA devices. The project aims at exploiting the possibility to partially modify the system affected by a SEU fault in order to mitigate the effects of such failures.

... and others (e.g., Blanket, HERA, HLR, Nomad, RDL, Valerie, ...).

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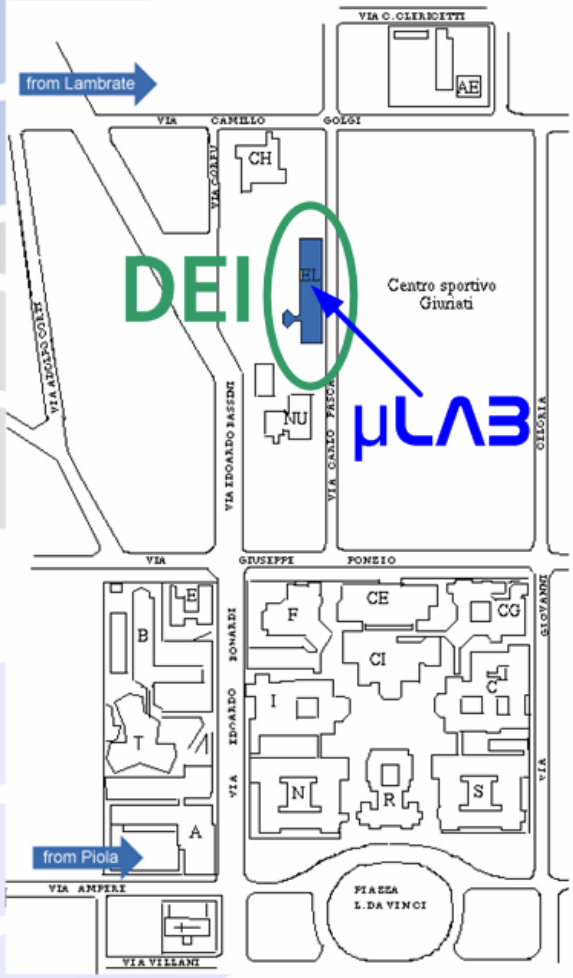

DRESD

Dynamic Reconfigurability in Embedded Systems Design

DRESD PHILOSOPHY:

Do or do not! There's no try!

Master Yoda

I need to believe that something extraordinary is possible!

Alicia Nash

DRESD

WHAT IS DRESD?:

DRESD is a research group that focuses on reconfigurable computing. DRESD can also be seen as a community that involves people coming from several universities and research facilities working on reconfigurable systems.

A BRIEF HISTORY OF DRESD:

DRESD was born at the **MicroArchitecture** (μΛ3) laboratory of the Politecnico di Milano, in 2004. Currently DRESD cooperate with several universities and companies, such as the Northwestern University, the Heinz Nixdorf Institute, the Ecole Polytechnique de Lausanne and Nokia Siemens Network, Synplicity, Impulse, Xilinx, ATMEL.

DRESD RATIONALE:

Over the last years, considerable interest has risen towards the field of reconfigurable hardware systems, with noteworthy research efforts in this direction. Especially interesting is the scenario in which this reconfiguration of the hardware is carried out without necessarily having to cease execution of those parts of the system that are not involved. The successful deployment of such complex and reconfigurable embedded systems to the market requires the identification, formalization, and implementation of concepts, methods, and tools that are able to ease the development of software components and the implementation of the system architecture. This scenario is the one in which the DRESD research project takes place.

DRESD OBJECTIVES:

Aims of the DRESD community are:

.:: The creation of an active discussion forum where all people involved in the reconfigurable computing area can find a place where to post their ideas, ask for problems and hopefully find solutions.

.:: A community full of life and interested not only in the reconfigurable computing area, but also in all those areas that are connected to that one i.e. Operating Systems, Compiler Design, Computer Architecture etc. etc.

.:: The definition of a methodology, for the design and development of a particular kind of embedded systems that exploit the advantages of dynamic reconfigurability.

.:: The creation of a strong connection between research, curricula in the academic world and industrial innovation.

HOW YOU CAN CONTRIBUTE:

There are several ways in which it is possible to collaborate with DRESD. First of all, it is possible to visit the official website (**www.dresd.org**) in order to better understand our research projects, or it is possible to have more information by writing to **info@dresd.org**

DRESD

WWW.DRESD.ORG